ABSTRACT OF THE DISCLOSURE

Methods and arrangements are provided for significantly reducing electron trapping in semiconductor devices having a polysilicon feature and an overlying dielectric layer. The methods and arrangements employ a nitrogen-rich region within the polysilicon feature near the interface to the overlying dielectric layer. The methods include selectively implanting nitrogen ions through at least a portion of the overlying dielectric layer and into the polysilicon feature to form an initial nitrogen concentration profile within the polysilicon feature. Next, the temperature within the polysilicon feature is raised to an adequately high temperature, for example using rapid thermal anneal (RTA) techniques, which cause the initial nitrogen concentration profile to change due to the migration of the majority of the nitrogen towards either the interface with the overlying dielectric layer or the interface with an underlying layer. Consequently, the polysilicon feature has a first nitrogen-rich region near the interface to the overlying dielectric layer and a second nitrogen-rich region near the interface to the underlying layer. The migration of nitrogen further forms a contiguous reduced-nitrogen region located between the first nitrogen-rich region and the second nitrogen-rich region. The contiguous reduced-nitrogen region has a lower concentration of nitrogen than does the first nitrogen-rich region and the second nitrogen-rich region. The first nitrogen-rich region has been found to reduce electron trapping within the polysilicon feature. Thus, for example, in a non-volatile memory device wherein the polysilicon feature is a floating gate, false programming of the memory device can be significantly avoided by reducing the number of trapped electrons in the floating gate.